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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/662,445	AGAN, MARTIN J.	
	Examiner	Art Unit	
	SELAM T. GEBRIEL	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01/15/2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *See Continuation Sheet* is/are pending in the application.

4a) Of the above claim(s) *40,42,43,65,68,91,112,113 and 116* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *31 - 39, 41, 46 - 48, 60, 61, 84 - 86, 88 - 90, 92, 107- 111, 114, 115, and 117* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Continuation of Disposition of Claims: Claims pending in the application are 31 - 43, 46 - 48, 60, 61, 64, 65, 68, 84 - 86, 88 - 92,107 - 117

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 31 – 39, 41, 46 – 48, 60, 61, 84 – 86, 88 – 90, 92 and 107 – 111, 114, 115, and 117 have been considered but are moot in view of the new ground(s) of rejection.

Election/Restrictions

2. Newly submitted claims 42, 43,112, 113, and 116 are directed to an invention that is independent or distinct from the invention originally claimed for the following reasons: Claims 42, 43, 112, 113, and 116 are directed to non-elected species 2 (Figure 5). Species 2 or Figure 5 pertains to a Five-Transistor (5T) pixel sensor cell including one transfer transistor and two reset transistor.

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 42, 43,112, 113, and 116 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Claim Objections

3. Claim 108 is objected to because it depends on itself. The examiner will assume as claim 108 depending on claim 107 for prosecution purpose.

4. Claim 41 line 4 the word "first" should be deleted. (Examiner talked with the applicant regarding the claim language and the applicant agreed to delete the word "first from claim language)

5. Claim 60 line 2 the word "first" should be deleted. (Examiner talked with the applicant regarding the claim language and the applicant agreed to delete the word "first from claim language)

Appropriate correction is needed.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 31 – 39, 41, 46 – 48, 60, 61, 84 – 86, 88 – 90, 92 and 107 – 111, 114, 115, and 117 are rejected under 35 U.S.C. 103(a) as being unpatentable over Compton (US 2004/0081446 A1) in view of Afghahi (US 2002/0030152 A1).

Regarding claim 31, Compton discloses a method of pixels in an array of an imaging device (Figure 2 and 5A – 5D Image sensor 90) comprising:

Opening a mechanical shutter (Page 2, Section 0019 and "FIG. 5a illustrates the initial position of the mechanical shutter 160 before image capture");

Resetting all pixels of an array to begin a first integration period (Page 2 Section 0019, the first row of pixels 180 is reset at time to and the other rows are reset sequentially after this. For example and referring to FIG. 5b, at time t.sub.1, the mechanical shutter 160 moves into the optical path of the first row of pixels 180 of the image sensor 90 which effectively stops the light measuring process by the pixels 180. This synchronization forms an exposure window between the leading edge 195 of the

mechanical shutter 160 and the last row pixels (for example row of pixels 190) that are reset for permitting each row of pixels in this window to be exposed to the light measuring process by resetting each row of pixels in a predetermined spatial relationship with the mechanical shutter for effectively creating an exposure time for the pixels. and Figure 5A, 5B and 5C, See the reset line, all rows of pixels are reset sequentially);

Accumulating charge in at least one photoconversion device of each pixel (Page 2 Section 0020, the mechanical shutter 160 is shown covering all the rows of pixels for illustrating that the exposure for all the pixels is complete and Figure 5B and 5C shows how the charges are being accumulated by the photodiodes, it is done by row by row manner and Figure 5D shows after all the photodiodes within the image sensor accumulated charge);

Closing the shutter to end the first integration period (Page 2 Section 0020, referring to FIG. 5d, the mechanical shutter 160 is shown covering all the rows of pixels for illustrating that the exposure for all the pixels is complete).

Resetting a charge collection region of each of the pixels to obtain a respective reset voltage for each pixel and reading out the reset voltage (Page 2 Section 0016, "To reset the photodiode 20, a reset gate 80 is activated for setting the floating diffusion 40 to a reference voltage, and the transfer gate 30 is activated substantially simultaneously for resetting the photodiode 20 to this reference voltage via the floating diffusion 40");

Transferring accumulated charge from each photoconversion device to an associated charge collection region of each pixel (Compton, Page 2 Section 0015 "A

transfer gate 30 is electrically connected to both the photodiode 20 and a floating diffusion 40, and the transfer gate 30 is activated for transferring the charge from the photodiode 20 to the floating diffusion 40"); and

Reading out the charge residing in each charge collection region to obtain a respective signal voltage for each pixel (Page 0015 "A transfer gate 30 is electrically connected to both the photodiode 20 and a floating diffusion 40, and the transfer gate 30 is activated for transferring the charge from the photodiode 20 to the floating diffusion 40. The charge is then passed to an output transistor 50 which is biased by voltage VDD, and as a result, the charge is converted to a voltage or signal, and this signal is passed to row select transistor 60. The row select transistor 60 is selectively activated for passing the signal to a common column line or bus 70 that passes the signal out of the pixel for further processing").

Compton does not disclose simultaneously resetting all pixels of an array to begin a first integration period.

Afghahi disclose pixel sensor array (Page 1 Section 0016) comprising a pixel cell 240 as shown in figure 2, wherein all the pixels of the array of which pixel 240 is a part are globally or simultaneously reset (Page 2 Section 0019).

Therefore it would have been obvious to one ordinary skilled in the art at the time the invention was made to modify the reset operation of the active pixel sensor taught by Compton with a well know reset method of global or simultaneous reset and as taught by Afghahi to simultaneously reset the photodiode of each pixels. The advantage of using the well known method of global or simultaneous reset and as taught by

Afghani is to control or reduce the amount of blur or ghosting images in the captured image by reducing the negative potential photographic effects of potential movement of objects within that picture frame of time while the image is taken.

Regarding claim 32, Compton in view of Afghahi disclose the method of claim 31, wherein the reset and signal voltages of the pixels are readout on a row by row basis after the mechanical shutter is closed and the first integration period ends (Compton, Page 2 Section 0016 "readout occurs after all the pixels 10 have been reset by activating the row select line 120 for a particular row, and consequently the row select transistors 60 for that particular row. All the rows of pixels 10 contain the reset line 100; transfer line 110 and row select line 120, although some are not shown").

Regarding claim 33, Compton discloses a technique of resetting all the pixels of the array by turning on a reset transistor and a transfer transistor within each pixel to couple the photo-conversion device of each pixel to a voltage source (Page 2 Section 0016, "To reset the photodiode 20, a reset gate 80 is activated for setting the floating diffusion 40 to a reference voltage, and the transfer gate 30 is activated substantially simultaneously for resetting the photodiode 20 to this reference voltage via the floating diffusion 40").

Compton does not disclose simultaneously resetting all the pixels of the array by turning on a reset transistor and a transfer transistor within each pixel to couple the photo-conversion device of each pixel to a voltage source.

Afghahi disclose pixel sensor array (Page 1 Section 0016) comprising a pixel cell 240 as shown in figure 2, wherein all the pixels of the array of which pixel 240 is a part are globally or simultaneously reset (Page 2 Section 0019).

Therefore it would have been obvious to one ordinary skilled in the art at the time the invention was made to modify the method of resetting the photodiodes in the active pixel sensor taught by Compton with a well know reset method of global or simultaneous reset and as taught by Afghahi to simultaneously reset the photodiode of each pixels. The advantage of using the well known method of global or simultaneous reset and as taught by Afghani is to control or reduce the amount of blur or ghosting images in the captured image by reducing the negative potential photographic effects of potential movement of objects within that picture frame of time while the image is taken.

Regarding claim 34, Compton in view of Afghahi further disclose the method of claim 33, wherein the reset transistor and **the** transfer transistor are turned on simultaneously to begin the first integration period (Compton, Page 2, Section 0015, To reset the photodiode 20, a reset gate 80 is activated for setting the floating diffusion 40 to a reference voltage, and the transfer gate 30 is activated substantially simultaneously for resetting the photodiode 20).

Regarding claim 35, Compton discloses a technique of resetting all the pixels of the array by turning on a reset transistor and a transfer transistor within each pixel to couple the photo-conversion device of each pixel to a voltage source (Page 2 Section 0016, "To reset the photodiode 20, a reset gate 80 is activated for setting the floating diffusion 40 to a reference voltage, and the transfer gate 30 is activated substantially

simultaneously for resetting the photodiode 20 to this reference voltage via the floating diffusion 40").

Compton does not disclose simultaneously resetting all the pixels of the array by turning on a reset transistor and a transfer transistor within each pixel to couple the photo-conversion device of each pixel to a voltage source.

Afghahi disclose pixel sensor array (Page 1 Section 0016) comprising a pixel cell 240 as shown in figure 2, wherein all the pixels of the array of which pixel 240 is a part are globally or simultaneously reset (Page 2 Section 0019).

Therefore it would have been obvious to one ordinary skilled in the art at the time the invention was made to modify the method of resetting the photodiodes in the active pixel sensor taught by Compton with a well know reset method of global or simultaneous reset and as taught by Afghahi to simultaneously reset the photodiode of each pixels. The advantage of using the well known method of global or simultaneous reset and as taught by Afghani is to control or reduce the amount of blur or ghosting images in the captured image by reducing the negative potential photographic effects of potential movement of objects within that picture frame of time while the image is taken.

Regarding claim 36, Compton in view of Afghahi further disclose the method of claim 31, wherein **the** image sensor is a CMOS image sensor (Compton, See Figure 1, 2, and 3).

Regarding claim 37, Compton in view of Afghahi further disclose the method of claim 31, wherein **the** charge collection region is a floating diffusion region (Compton, Page 2 Section 0015, A floating diffusion 40 is used for collecting charges).

Regarding claim 38, Compton in view of Afghahi further disclose the method of claim 37, wherein **the** act of reading out the reset voltage comprises reading out the reset voltage from **the** floating diffusion region (Compton, Page 0015 "A transfer gate 30 is electrically connected to both the photodiode 20 and a floating diffusion 40, and the transfer gate 30 is activated for transferring the charge from the photodiode 20 to the floating diffusion 40. The charge is then passed to an output transistor 50 which is biased by voltage VDD, and as a result, the charge is converted to a voltage or signal, and this signal is passed to row select transistor 60. The row select transistor 60 is selectively activated for passing the signal to a common column line or bus 70 that passes the signal out of the pixel for further processing").

Regarding claim 39, Compton in view of Afghahi further disclose the method of claim 31, wherein the pixel comprises four transistors (Compton, See Figure 1, Reset, Select, Transfer and Output Transistors).

Regarding claim 117, Compton in view of Afghahi further disclose the method of claim 31, wherein transferring accumulated charge from each photoconversion device to an associated charge collection region of each pixel comprises operating a transfer transistor associated with each photoconversion device of each pixel (Compton, Page 2 Section 0015 "A transfer gate 30 is electrically connected to both the photodiode 20 and a floating diffusion 40, and the transfer gate 30 is activated for transferring the charge from the photodiode 20 to the floating diffusion 40").

Regarding claim 107, Compton disclose a method of operating an imaging device (Figure 2 and 5A – 5D Image sensor 90) comprising:

Opening a mechanical shutter (Page 2, Section 0019 and "FIG. 5a illustrates the initial position of the mechanical shutter 160 before image capture");

Resetting all pixels of an array to begin a first integration period (Page 2 Section 0019, the first row of pixels 180 is reset at time to and the other rows are reset sequentially after this. For example and referring to FIG. 5b, at time t.sub.1, the mechanical shutter 160 moves into the optical path of the first row of pixels 180 of the image sensor 90 which effectively stops the light measuring process by the pixels 180. This synchronization forms an exposure window between the leading edge 195 of the mechanical shutter 160 and the last row pixels (for example row of pixels 190) that are reset for permitting each row of pixels in this window to be exposed to the light measuring process by resetting each row of pixels in a predetermined spatial relationship with the mechanical shutter for effectively creating an exposure time for the pixels. and Figure 5A, 5B and 5C, See the reset line, all rows of pixels are reset sequentially);

Accumulating charge in at least one photoconversion device of each pixel (Page 2 Section 0020, the mechanical shutter 160 is shown covering all the rows of pixels for illustrating that the exposure for all the pixels is complete and Figure 5B and 5C shows how the charges are being accumulated by the photodiodes, it is done by row by row manner and Figure 5D shows after all the photodiodes within the image sensor accumulated charge);

Closing the shutter to end the first integration period (Page 2 Section 0020, referring to FIG. 5d, the mechanical shutter 160 is shown covering all the rows of pixels for illustrating that the exposure for all the pixels is complete).

Compton does not disclose simultaneously resetting all pixels of an array to begin a first integration period.

Afghahi disclose pixel sensor array (Page 1 Section 0016) comprising a pixel cell 240 as shown in figure 2, wherein all the pixels of the array of which pixel 240 is a part are globally or simultaneously reset (Page 2 Section 0019).

Therefore it would have been obvious to one ordinary skilled in the art at the time the invention was made to modify the reset operation of the active pixel sensor taught by Compton with a well know reset method of global or simultaneous reset and as taught by Afghahi to simultaneously reset the photodiode of each pixels. The advantage of using the well known method of global or simultaneous reset and as taught by Afghani is to control or reduce the amount of blur or ghosting images in the captured image by reducing the negative potential photographic effects of potential movement of objects within that picture frame of time while the image is taken.

Regarding claim 108, Compton in view of Afghahi disclose the method of claim 108, wherein the signal voltages of the pixels are readout on a row by row basis after the mechanical shutter (Figure 5A – 5D mechanical shutter 160) is closed and the first integration period ends (Compton, Page 2 Section 0016 "readout occurs after all the pixels 10 have been reset by activating the row select line 120 for a particular row, and consequently the row select transistors 60 for that particular row. All the rows of pixels

10 contain the reset line 100; transfer line 110 and row select line 120, although some are not shown").

Regarding claim 109, Compton in view of Afghahi further disclose the method of claim 107, further comprising transferring accumulated charge from each photoconversion device to an associated charge collection region of each pixel by operating a transfer transistor of each pixel (Compton, Page 2 Section 0015 "A transfer gate 30 is electrically connected to both the photodiode 20 and a floating diffusion 40, and the transfer gate 30 is activated for transferring the charge from the photodiode 20 to the floating diffusion 40").

Regarding claim 110, Compton in view of Afghahi further disclose the method of claim 109, further comprising reading out the charge residing in each charge collection region to obtain a respective signal voltage for each pixel (Compton, Page 0015 "A transfer gate 30 is electrically connected to both the photodiode 20 and a floating diffusion 40, and the transfer gate 30 is activated for transferring the charge from the photodiode 20 to the floating diffusion 40. The charge is then passed to an output transistor 50 which is biased by voltage VDD, and as a result, the charge is converted to a voltage or signal, and this signal is passed to row select transistor 60. The row select transistor 60 is selectively activated for passing the signal to a common column line or bus 70 that passes the signal out of the pixel for further processing").

Regarding claim 111, Compton in view of Afghahi further disclose the method of claim 110, wherein the charge collection region is a floating diffusion region (Compton, Page 2 Section 0015, A floating diffusion 40 is used for collecting charges).

Regarding claim 114, Compton discloses a technique of resetting all the pixels of the array by turning on a reset transistor and a transfer transistor within each pixel to couple the photo-conversion device of each pixel to a voltage source (Page 2 Section 0016, "To reset the photodiode 20, a reset gate 80 is activated for setting the floating diffusion 40 to a reference voltage, and the transfer gate 30 is activated substantially simultaneously for resetting the photodiode 20 to this reference voltage via the floating diffusion 40").

Compton does not disclose simultaneously resetting all the pixels of the array by turning on a reset transistor and a transfer transistor within each pixel to couple the photo-conversion device of each pixel to a voltage source.

Afghahi disclose pixel sensor array (Page 1 Section 0016) comprising a pixel cell 240 as shown in figure 2, wherein all the pixels of the array of which pixel 240 is a part are globally or simultaneously reset (Page 2 Section 0019).

Therefore it would have been obvious to one ordinary skilled in the art at the time the invention was made to modify the method of resetting the photodiodes in the active pixel sensor taught by Compton with a well know reset method of global or simultaneous reset and as taught by Afghahi to simultaneously reset the photodiode of each pixels. The advantage of using the well known method of global or simultaneous reset and as taught by Afghani is to control or reduce the amount of blur or ghosting images in the captured image by reducing the negative potential photographic effects of potential movement of objects within that picture frame of time while the image is taken.

Regarding claim 115, Compton in view of Afghahi further disclose the method of claim 107, wherein each pixel (Figure 1) comprises four transistors (Compton, See Figure 1, Reset, Select, Transfer and Output Transistors).

Regarding claim 117, Compton in view of Afghahi further disclose the method of claim 31, wherein transferring accumulated charge from each photoconversion device to an associated charge collection region of each pixel comprises operating a transfer transistor associated with each photoconversion device of each pixel (Compton, Page 2 Section 0015 "A transfer gate 30 is electrically connected to both the photodiode 20 and a floating diffusion 40, and the transfer gate 30 is activated for transferring the charge from the photodiode 20 to the floating diffusion 40").

Regarding claim 41, Compton discloses an imaging device (Figure 1, 2 and 5A – 5D Image sensor 90) comprising: an array of pixels (Figure 2), each pixel (Figure 1) comprising:

A photoconversion device (Figure 1, Photodiode 20) for accumulating charge (Page 2, Section 0015 and 0016),

A first reset transistor (Figure 1 and 2 reset gate 80) for resetting the photoconversion device (Page 2, Section 0015, To reset the photodiode 20, a reset gate 80 is activated for setting the floating diffusion 40 to a reference voltage, and the transfer gate 30 is activated substantially simultaneously for resetting the photodiode 20);

A charge collection region (Figure 1 and 2 Floating region 40) for receiving the charge from the photoconversion device (Page 2, Section 0015, the charge collection

region or the floating region 40 is reset by a reset gate 50 and receives charge from the photoconversion device), and

A transfer transistor (Figure 1 and 2 Transfer gate 30) for transferring charge from the photoconversion device to the charge collection region (Page 2 Section 0015 "A transfer gate 30 is electrically connected to both the photodiode 20 and a floating diffusion 40, and the transfer gate 30 is activated for transferring the charge from the photodiode 20 to the floating diffusion 40"), and

A readout circuit (Figure 1, Processor 150) for reading out the charge from the charge collection region, (Page 2, Section 0015, The charge is then passed to an output transistor 50 which is biased by voltage VDD, and as a result, the charge is converted to a voltage or signal, and this signal is passed to row select transistor 60. The row select transistor 60 is selectively activated for passing the signal to a common column line or bus 70 that passes the signal out of the pixel for further processing and Page 2 Section 0016 "readout occurs after all the pixels 10 have been reset by activating the row select line 120 for a particular row, and consequently the row select transistors 60 for that particular row. All the rows of pixels 10 contain the reset line 100; transfer line 110 and row select line 120, although some are not shown").

A mechanical shutter (Page 2, Section 0016 and 0019, See Figure 5A – 5D Mechanical shutter 160);

A timing and control circuit (Figure 1, Processor 150 and Mechanical Shutter Actuator 170) configured to open the mechanical shutter and close the mechanical shutter to end said integration period (Page 2 Section 0017).

Compton does not disclose simultaneously operate each first reset transistor to reset the photoconversion devices in all pixels of the array to begin an integration period

Afghahi disclose pixel sensor array (Page 1 Section 0016) comprising a pixel cell 240 as shown in figure 2, wherein all the pixels of the array of which pixel 240 is a part are globally or simultaneously reset by Programmable circuit 236 and Voltage regulator 238 (Page 2 Section 0019).

Therefore it would have been obvious to one ordinary skilled in the art at the time the invention was made to modify the reset operation of the active pixel sensor taught by Compton with a well know reset method of global or simultaneous reset and as taught by Afghahi to simultaneously reset the photodiode of each pixels. The advantage of using the well known method of global or simultaneous reset and as taught by Afghani is to control or reduce the amount of blur or ghosting images in the captured image by reducing the negative potential photographic effects of potential movement of objects within that picture frame of time while the image is taken.

Regarding claim 46, Compton in view of Afghahi further disclose the imaging device of claim 41, wherein the timing and control circuit (Figure 1 Processor 150) is further configured to cause a reset voltage from each pixel to be readout in a row by row manner after the shutter is closed (Compton, Page 2 Section 0016 "readout occurs after all the pixels 10 have been reset by activating the row select line 120 for a particular row, and consequently the row select transistors 60 for that particular row. All the rows of pixels 10 contain the reset line 100; transfer line 110 and row select line 120, although some are not shown").

Regarding claim 47, Compton in view of Afghahi further disclose the imaging device of claim 46, wherein the timing and control circuit (Figure 1 Processor 150) is further configured to cause a signal voltage from each pixel to be readout in a row by row manner after the reset voltage is readout (Compton, Page 2 Section 0016 "readout occurs after all the pixels 10 have been reset by activating the row select line 120 for a particular row, and consequently the row select transistors 60 for that particular row. All the rows of pixels 10 contain the reset line 100; transfer line 110 and row select line 120, although some are not shown").

Regarding claim 48, Compton in view of Afghahi further disclose the imaging device of claim 41, wherein each pixel (Figure 1) comprises four transistors (Compton, See Figure 1, Reset, Select, Transfer and Output transistors).

Regarding claim 60, Compton discloses a timing control circuit (Figure 3, Processor 150) for an imager array (Figure 2 and Figure 5A – 5D) comprising:

Circuitry (Figure 3, Processor 150 and Mechanical Shutter Actuator 170) for applying a first driving voltage to operate at least one transistor of the array, to reset a photoconversion device of each respective pixel to a predetermined voltage to begin an integration period during which each photoconversion device collects charge in response to incident light (Page 2 Section 0019, the first row of pixels 180 is reset at time to and the other rows are reset sequentially after this. For example and referring to FIG. 5b, at time t.sub.1, the mechanical shutter 160 moves into the optical path of the first row of pixels 180 of the image sensor 90 which effectively stops the light measuring process by the pixels 180. This synchronization forms an exposure window between the

leading edge 195 of the mechanical shutter 160 and the last row pixels (for example row of pixels 190) that are reset for permitting each row of pixels in this window to be exposed to the light measuring process by resetting each row of pixels in a predetermined spatial relationship with the mechanical shutter for effectively creating an exposure time for the pixels. And Figure 5A, 5B and 5C, See the reset line, all rows of pixels are reset sequentially).

Circuitry (Figure 3, Processor 150 and Mechanical Shutter Actuator 170) for closing mechanical shutter to end the integration period (See Figure 5A – 5D, Figure 5D us when the mechanical shutter is closed and integration ends); and

circuitry (Figure 3, Processor 150) for causing the charge to read out from each photoconversion device of each pixel in a row by row manner (Page 2, Section 0015, The charge is then passed to an output transistor 50 which is biased by voltage VDD, and as a result, the charge is converted to a voltage or signal, and this signal is passed to row select transistor 60. The row select transistor 60 is selectively activated for passing the signal to a common column line or bus 70 that passes the signal out of the pixel for further processing and Page 2 Section 0016 "readout occurs after all the pixels 10 have been reset by activating the row select line 120 for a particular row, and consequently the row select transistors 60 for that particular row. All the rows of pixels 10 contain the reset line 100; transfer line 110 and row select line 120, although some are not shown").

Compton does not disclose simultaneously resetting all pixels of an array to begin a first integration period.

Afghahi disclose pixel sensor array (Page 1 Section 0016) comprising a pixel cell 240 as shown in figure 2, wherein all the pixels of the array of which pixel 240 is a part are globally or simultaneously reset (Page 2 Section 0019).

Therefore it would have been obvious to one ordinary skilled in the art at the time the invention was made to modify the reset operation of the active pixel sensor taught by Compton with a well know reset method of global or simultaneous reset and as taught by Afghahi to simultaneously reset the photodiode of each pixels. The advantage of using the well known method of global or simultaneous reset and as taught by Afghani is to control or reduce the amount of blur or ghosting images in the captured image by reducing the negative potential photographic effects of potential movement of objects within that picture frame of time while the image is taken.

Regarding claim 61, Compton in view of Afghahi further disclose the circuit of claim 60, wherein the circuitry (Compton, Figure 3, Processor 150) for applying the first driving voltage applies the driving voltage to a reset transistor and a transfer transistor of each pixel of the array (Compton, Page 2, Section 0015, To reset the photodiode 20, a reset gate 80 is activated for setting the floating diffusion 40 to a reference voltage, and the transfer gate 30 is activated substantially simultaneously for resetting the photodiode 20).

Regarding claim 84, Compton discloses an imager device (Figure 2 and Figure 5A – 5D) comprising:

A pixel array (Figure 2) comprising:

A plurality of pixels (Figure 2, Pixels 10);

Readout circuitry (Figure 3, Processor 150) for the array (Page 2, Section 0015, The charge is then passed to an output transistor 50 which is biased by voltage VDD, and as a result, the charge is converted to a voltage or signal, and this signal is passed to row select transistor 60. The row select transistor 60 is selectively activated for passing the signal to a common column line or bus 70 that passes the signal out of the pixel for further processing and Page 2 Section 0016 "readout occurs after all the pixels 10 have been reset by activating the row select line 120 for a particular row, and consequently the row select transistors 60 for that particular row. All the rows of pixels 10 contain the reset line 100; transfer line 110 and row select line 120, although some are not shown");

A mechanical shutter (Figure 1 and 5A – 5D, Mechanical Shutter 160) for ending the integration period when the mechanical shutter is moved from an open position to a closed position (Page 2, Section 0016, 0017 and 0019, and 0020, See Figure 5A – 5D).

Global circuitry (Figure 3, Processor 150) for resetting a photoconversion device of each of the array to begin an integration period (Page 2 Section 0019, the first row of pixels 180 is reset at time to and the other rows are reset sequentially after this. For example and referring to FIG. 5b, at time t.sub.1, the mechanical shutter 160 moves into the optical path of the first row of pixels 180 of the image sensor 90 which effectively stops the light measuring process by the pixels 180. This synchronization forms an exposure window between the leading edge 195 of the mechanical shutter 160 and the last row pixels (for example row of pixels 190) that are reset for permitting each row of pixels in this window to be exposed to the light measuring process by resetting each

row of pixels in a predetermined spatial relationship with the mechanical shutter for effectively creating an exposure time for the pixels and Figure 5A, 5B and 5C, See the reset line, all rows of pixels are reset sequentially); and

Compton does not disclose simultaneously resetting all pixels of an array to begin a first integration period.

Afghahi disclose pixel sensor array (Page 1 Section 0016) comprising a pixel cell 240 as shown in figure 2, wherein all the pixels of the array of which pixel 240 is a part are globally or simultaneously reset (Page 2 Section 0019).

Therefore it would have been obvious to one ordinary skilled in the art at the time the invention was made to modify the reset operation of the active pixel sensor taught by Compton with a well know reset method of global or simultaneous reset and as taught by Afghahi to simultaneously reset the photodiode of each pixels. The advantage of using the well known method of global or simultaneous reset and as taught by Afghani is to control or reduce the amount of blur or ghosting images in the captured image by reducing the negative potential photographic effects of potential movement of objects within that picture frame of time while the image is taken.

Regarding claim 85, Compton in view of Afghahi further disclose the device of claim 84, wherein the readout circuitry (Figure 3 Processor 150) is configured to read out the pixels on a row by row basis after the mechanical shutter is closed and the first integration period ends (Compton, Page 2, Section 0015, The charge is then passed to an output transistor 50 which is biased by voltage VDD, and as a result, the charge is converted to a voltage or signal, and this signal is passed to row select transistor 60.

The row select transistor 60 is selectively activated for passing the signal to a common column line or bus 70 that passes the signal out of the pixel for further processing and Page 2 Section 0016 "readout occurs after all the pixels 10 have been reset by activating the row select line 120 for a particular row, and consequently the row select transistors 60 for that particular row. All the rows of pixels 10 contain the reset line 100; transfer line 110 and row select line 120, although some are not shown").

Regarding claim 86, Compton discloses a processor 150 and Mechanical Shutter Actuator 170 for resetting all the pixels of the array by turning on a reset transistor and a transfer transistor within each pixel to couple the photo-conversion device of each pixel to a voltage source. (Page 2 Section 0016, "To reset the photodiode 20, a reset gate 80 is activated for setting the floating diffusion 40 to a reference voltage, and the transfer gate 30 is activated substantially simultaneously for resetting the photodiode 20 to this reference voltage via the floating diffusion 40").

Compton does not disclose the processor 150 and mechanical shutter actuator for simultaneously resetting all the pixels of the array by turning on a reset transistor and a transfer transistor within each pixel to couple the photo-conversion device of each pixel to a voltage source.

Afghahi disclose pixel sensor array (Page 1 Section 0016) comprising a pixel cell 240 as shown in figure 2, wherein all the pixels of the array of which pixel 240 is a part are globally or simultaneously reset by programmable circuit 236 and voltage regulator 238 (Page 2 Section 0019).

Therefore it would have been obvious to one ordinary skilled in the art at the time the invention was made to modify the method of resetting the photodiodes in the active pixel sensor taught by Compton with a well know reset method of global or simultaneous reset and as taught by Afghahi to simultaneously reset the photodiode of each pixels. The advantage of using the well known method of global or simultaneous reset and as taught by Afghani is to control or reduce the amount of blur or ghosting images in the captured image by reducing the negative potential photographic effects of potential movement of objects within that picture frame of time while the image is taken.

Regarding claim 88, Compton in view of Afghahi further disclose the device of claim 84, wherein the readout circuitry (Compton, Figure 3 Processor 150) comprises circuitry for reading out reset voltages and output voltages for the plurality of pixels (Compton, Page 2, Section 0015, The charge is then passed to an output transistor 50 which is biased by voltage VDD, and as a result, the charge is converted to a voltage or signal, and this signal is passed to row select transistor 60. The row select transistor 60 is selectively activated for passing the signal to a common column line or bus 70 that passes the signal out of the pixel for further processing and Page 2 Section 0016 "readout occurs after all the pixels 10 have been reset by activating the row select line 120 for a particular row, and consequently the row select transistors 60 for that particular row. All the rows of pixels 10 contain the reset line 100; transfer line 110 and row select line 120, although some are not shown").

Regarding claim 89, Compton in view of Afghahi further disclose the device of claim 84, wherein the global circuitry (Compton Figure 3 Processor 150) for resetting

the photoconversion devices (2 Photodiodes 20) comprises circuitry for coupling the photoconversion device to a voltage source (Compton, Page 2, Section 0015, To reset the photodiode 20, a reset gate 80 is activated for setting the floating diffusion 40 to a reference voltage, and the transfer gate 30 is activated substantially simultaneously for resetting the photodiode 20).

Regarding claim 90, Compton in view of Afghahi further disclose the device of claim 89, wherein the photoconversion device (Figure 1 and 2 Photodiode 20) is coupled to a voltage source through a reset transistor (Compton, See figure 1, VDD and Photodiode 20 are connected through the reset gate 80).

Regarding claim 92, Compton in view of Afghahi further disclose the device of claim 90, wherein the photoconversion device is coupled to the voltage source through the reset transistor (Figure 1 reset gate 50) and a transfer transistor (Figure 1 transfer gate 30) which transfers accumulated charge from the photoconversion device (Compton, See Figure 1, VDD and Photodiode 20 are connected through the reset gate 80 and the transfer gate 30).

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date

the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contacts

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SELAM T. GEBRIEL whose telephone number is (571)270-1652. The examiner can normally be reached on Monday-Thursday 8:30 am to 5.00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tran Sinh can be reached on 571-272-7564.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Selam T Gebriel/
Examiner, Art Unit 2622

Tuesday, March 31, 2009

/JOHN M. VILLECCO/
Primary Examiner, Art Unit 2622
April 7, 2009